FSK Demodulator- Case Study of PLL Application

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Abstract— *FSK Demodulator, one of the applications of PLL has been implemented using both hardware and software. Results are found to be similar and based on these results it is believed that this will contribute for the improvement in performance and reliability for future communication systems. Hence this will also contribute to the development of higher reliability of the systems.*

Keywords— implementation, contribute, improvement reliability,

I. INTRODUCTION

An early description of phase-locked loop (PLL) appeared in the papers by Appleton [l] in 1923 and deBellescize [2] in 1932. Weakening the use of Doppler shift effect, the advent of PLL has contributed to coherent communication systems. In the late 1970's, the theoretical description of PLL was well established [3], [4], [5], but PLL did not achieve widespread use until much later because of the difficulty in realization. With the rapid development of integrated circuits(IC's) in the 1970's, the applications of PLL were widely used in modem communication systems. Since then, the use of PLL has seen a substantial progress when compared with its earlier professional use in high-precision apparatuses into its current use in consumers' electronic products which has made much progress. To improve performance and reliability, especially in common electronic appliances that will be used daily, it has enabled modern electronic systems. In the 1970's, researchers in the control field first plaid attention to the realization of PLL for a synchronous motor speed control system [6]. Since then, Analog PLL IC's [7]-[15] were used in developing phase-locked servo systems (PLS's) for ac and dc motors' servomechanisms. Over the past 10 years, the rapidly developed high-performance digital IC's and microprocessors have strongly motivated the implementation of PLS using digital technology. This has led to the development of new types of controllers with added PLS features for achieving an easy-use and easy-control nature for ac and dc servo drives [11], [16]-[19], **[**20**],** [21].

II. COMPOSITION AND PRINCIPLE OF DIGITAL PLL

To control frequency and phase of the oscillator signal within control loop, PLL (phase-locked loop) which is a feedback control unit uses an external input reference signal. PLL is usually applied in closed-loop tracking phase-locked loop circuit, for that frequency of output signal can auto-track the frequency of input signal. During the process, when the input and output signal phases are approaching to be consistent, we say that phase-locked loop is running in traction and showing its transient characteristics; when the input and output signal phases remains the same, we say phase-locked loop into locked state and in steady status;. A typical PLL is usually composed of phase detector (PD), loop filter (LF) and voltage-controlled oscillators (VCO), shown in Fig.1.

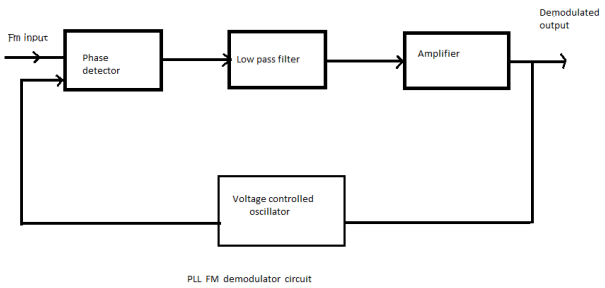


Fig. 1 Basic FM Demodulator circuit

Because the main difference of phase-locked loop and frequency-locked loop is phase detector, this paper gives the principle of phase-locked loop in the following introduction.

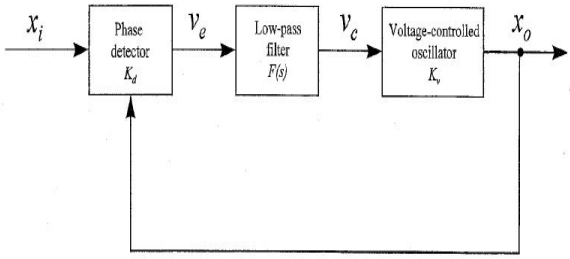


Fig. 2 Block Diagram of Phase Locked Loop

2.1 Phase detector [PD]

Sinusoidal PD's and the square signal PD's are basically the two types of PD's available. A sinusoidal PD

inherently has phase detection interval (-7r/2, +7r/2) which operates as a multiplier and is a zero memory device. The square signal PD's, also called sequential PD's, are implemented by sequential logic circuits. Generating PD characteristics that are difficult or impossible to obtain with multiplier circuits are generated by using these Sequential PD's which contain memory of past events. They are usually built up from digital circuits and operate with binary rectangular input waveforms. And hence the name called digital phase detectors. The characteristics of the square signal PD's are of the linear type over the phase detection interval ($-\pi/2$, $+\pi/2$) for triangular PD, ($-\pi$, $+\pi$) for saw tooth PD, and (-2π, $+2\pi$) for sequential phase/frequency detector (PFD) [22], [23], [24], [25], [26], [27]. Their characteristics are depicted in Fig. 2 [28]. All curves of Fig. 3 are shown with the same slope at phase error = final phase-initial phase, = 0, which means that the different PD's all have the same factor *Kd*. Increasing PD phase detection interval provides a larger tracking range, larger lock limit, than those obtainable from a sinusoidal PD.

2.2 Voltage-Controlled Oscillator

Voltage-controlled oscillators, which in short called as VCO's are used in the PLL. Basically these are not different from those employed for other applications, such as modulation and automatic frequency control. There are some crucial requirements for VCO which are 1) phase stability, 2) large frequency deviation, 3) high modulation sensitivity *K*, 4) linearity of frequency versus control voltage, and 5) capability for accepting wide-band modulation. These are the four types of VCO's that are commonly used in the order of decreasing stability, namely, voltage controlled crystal oscillators (VCXO's), resonator oscillators, RC multivibrators, and YIG-tuned oscillators [37], [38]. The phase stability can be enhanced by a number of ways: 1) using high Q crystal and circuit, 2) maintaining low noise in the amplifier portion, 3) stabilizing temperature, and 4) keeping mechanical stability. An LC oscillator must be used, if a wider frequency range is required. The standard Hartley, Colpitts, and Clapp circuits make their appearance in this application. A varactor, junction capacitance of a diode are used to accomplish the tuning.

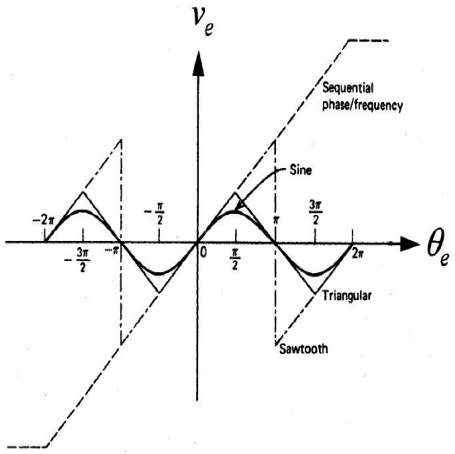


Fig. 2. Characteristics of the phase detector (taken from [4]).

Fig. 3 Characteristics of Phase Detector

2.3 Loop Filter

The low-pass filter indicated in the figure is nothing but the Loop Filter. This is used to suppress the noise and the high-frequency components from the PD and provide a dc-controlled signal for the VCO. And hence the filtering results not only reflects the phase changing of the filter input signal, but also avoids extremely regulating voltage controlled oscillator occurring because of noise. Loop filter design is mainly discussed in this paper. There are quite a few ranges in which the PLL can be defined as shown in the figure below.

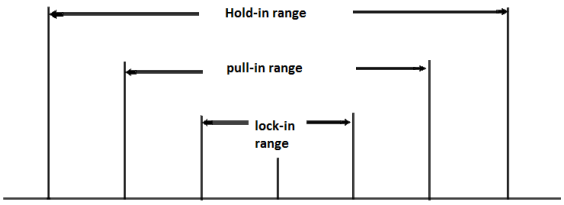


Fig. 4 Different ranges that are defined in PLL

III. SOFTWARE & HARDWARE IMPLEMENTATION OF FSK

In our project we have implemented the PLL in software by writing a Matlab code. The code that is implemented in the software is as shown below

1) First step is to give the basic input commands
   Clear all;
   Close all;
   f=1000; %Carrier frequency
   fs=100000; %Sample frequency
   N=5000; %Number of samples
   Ts=1/fs;
   t= (0: Ts :(N*Ts) - Ts);
2) Second step is to create the message signal and

the real, imaginary parts of a CW modulated carrier to be tracked.

```
%Create the message signal
f1=100; %Modulating frequency
msg= sin (2*pi*f1*t);
kf=.0628; %Modulation index
%Create the real and imaginary parts of a CW modulated
carrier to be tracked.
Signal=exp (j*(2*pi*f*t+2*pi*kf*cumsum (msg)));
Signal1=exp (j*(2*pi*f*t));
```

3) Now initializing the PLL loop and loop filter parameters.

```
%Initialize PLL Loop
M (1) =30;
e (1) =0;
N (1) =0;
vco (1) =0;
%Define Loop Filter parameters (Sets damping)
kp=0.15; %Proportional constant
ki=0.1; %Integrator constant
```

4) Finally implementing the PLL and plotting the waveforms.

```
for n=2: length (Signal)
vco (n) =conj (exp (j*(2*pi*n*f/fs+M (n-1))));
N (n) =imag (Signal (n)*vco (n));
e (n) =e (n-1) + (kp+ki)*N (n)-ki*N (n-1);
M (n) =M (n-1) +e (n); %Update VCO
end;
%Plot waveforms
startplot = 1;
endplot = 1000;
```

5) Now looking into the figures

```
figure (1);
subplot (3, 2,1);
plot(t(startplot:endplot), msg(startplot:endplot));
title('100 Hz message signal');
%xlabel('Time (seconds)');
ylabel('Amplitude');
grid;

figure(1);
subplot(3,2,2);
plot(t(startplot:endplot), real(Signal(startplot:endplot)));
title('FM (1KHz carrier modulated with a 100 Hz message
signal)');
%xlabel('Time (seconds)');
ylabel('Amplitude');
grid;

figure(1)
subplot(3,2,3);
plot(t(startplot:endplot), e(startplot:endplot));
title('PLL Loop Filter/Integrator Output');
%xlabel('Time (seconds)');
ylabel('Amplitude');
grid;
```

6) Referring to all the subplots which will be there in the output of the PLL implementation.

```
subplot(3,2,4);
plot(t(startplot:endplot), real(vco(startplot:endplot)));
title('VCO Output (PLL tracking the input signal)');
%xlabel('Time (seconds)');
ylabel('Amplitude');
grid;

subplot(3,2,5);
plot(t(startplot:endplot), phd_output(startplot:endplot));
title('Phase Detecter Output');
xlabel('Time (seconds)');
ylabel('Amplitude');
grid;

subplot(3,2,6);
plot(t(startplot:endplot), real(Signal1(startplot:endplot)));
title('Unmodulated Carrier');
xlabel('Time (seconds)');
ylabel('Amplitude');
grid;

figure(1);
subplot(3,2,1);
plot(t(startplot:endplot), msg(startplot:endplot));
title('100 Hz message signal');
%xlabel('Time (seconds)');
ylabel('Amplitude');
grid;

figure(1);
subplot(3,2,2);
plot(t(startplot:endplot), real(Signal(startplot:endplot)));
title('FM (1KHz carrier modulated with a 100 Hz message
signal)');
%xlabel('Time (seconds)');
ylabel('Amplitude');
grid;

figure(1)
subplot(3,2,3);
plot(t(startplot:endplot), e(startplot:endplot));
title('PLL Loop Filter/Integrator Output');
```

```
%xlabel('Time (seconds)');
ylabel('Amplitude');
grid;
```

The Output that we're arrived with would be a reference that PLL has been executed with absolute perfection. The output for the matlab code shown above will look like:

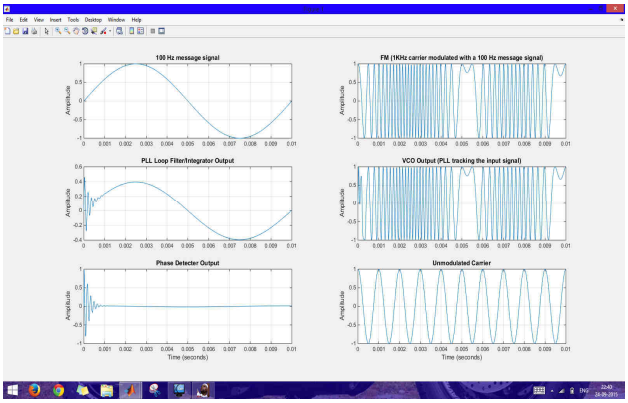
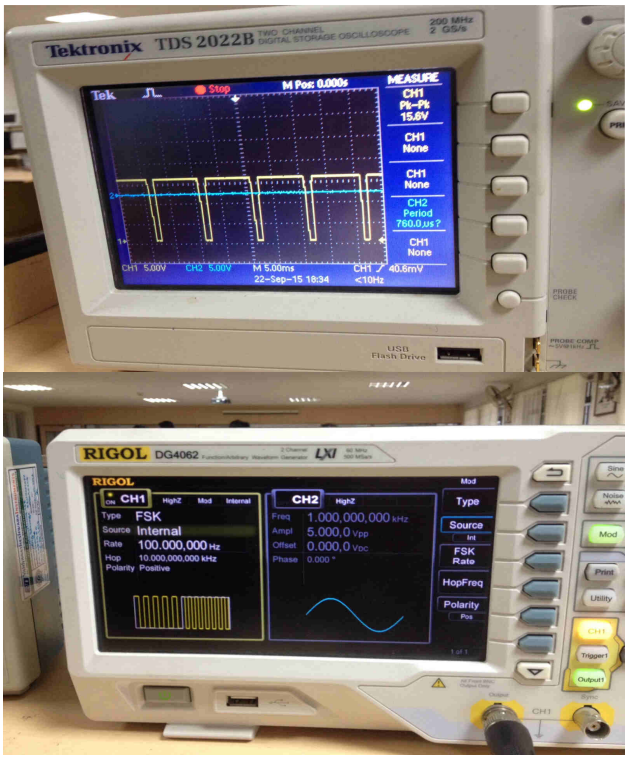


Fig. 5 Output Observed after the Implementation in Software

And the Circuit that has been constructed by using the hardware available would bring you almost the same results that you are obtained with in using the software. The circuit constructed and the output obtained would look like:



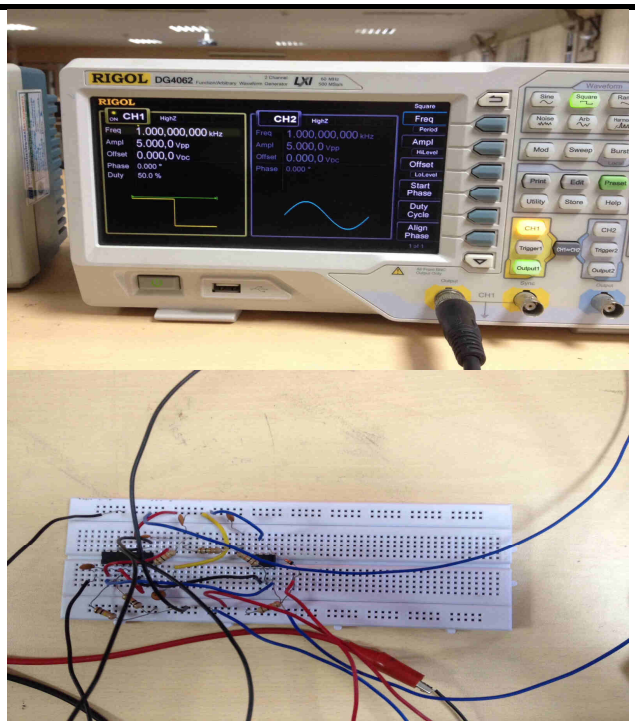


Fig. 6 Hardware Implementation of FSK Demodulation

IV. CONFIGURATIONS OF PLL APPLICATIONS

Integrated PLL's developed since the 1970's are versatile systems. For the use in a variety of frequency-selective demodulation, signal conditioning, or frequency-synthesis applications these are suitable. PLL techniques in communication are well developed and widely used for FM, AM, video, signal processing, telecommunication systems, etc. Due to its inherent configuration, PLL is frequently realized as a signal modulator or synthesizer. Using the PLL with analog PLL IC's (NE565 developed by Signetics) for a motor design began in the 1970's [29]-[35], [36]. Tracking the phase and frequency of the incoming reference signal that corresponds to the input command, such as speed or position and maintaining that continuously is done by a frequency feedback control configuration, which is called a PLS.

V. POPULAR PLL INTEGRATED CIRCUITS (IC'S)

A Sweeping variety of IC's for PLL are available from semiconductor manufacturers. Transistor-transistor logic (TTL), complementary metal-oxide-semiconductor (CMOS), and emitter coupled logic (ECL) are used in implementing the PLL. These days, fully integrated PLL on a single chip can operate at frequencies up to 35 MHz, such as Exar XR-215 PLL. Combination of sub-PLL IC's (including only PD, prescaler, and programmable counter) and discrete higher frequency VCO's are used in achieving the higher frequency PLL's. It is an important trend to realize that by constituting a high-frequency VCO into a modulus device in the near future a fully integrated higher frequency PLL. Versatile PLL IC's

operating at frequencies above 2.5 GHz are being developed by Motorola and Plessey, nowadays. A 2.5-GHz bipolar monolithic series-input phase locked loop synthesizer with phase-swallow function is nothing but the Motorola MC 12210. This is designed for the high-frequency local oscillator of an RF transceiver in handheld communication applications. These kind of PLL IC's can operate at a minimum supply voltage of 2.7 V for input frequencies up to 2.5 GHz with a typical current drain of 9.5 mA. And these PLL synthesizers operate at a low power consumption *(5* V and 30 mA).

VI. CONCLUSION

This paper has given a concise review of the PLL technique, which is applicable to communication and servo control systems. PLL circuit has been implemented using both the software and hardware and the results are found to be in accordance with each other. PLL technology's status and its applications have been discussed and also had a look into it's development trends. It is pointed out that the development of better PLL technology and the associated modular IC's is continuing.

REFERENCES

[1] E. V. Appleton, "Automatic synchronization of triode oscillators," in *Proc. Cambridge Phil. Soc.*, vol. 21, pt. 111, p. 231, 1922-1923.

[2] H. de Bellescize, "La reception synchrone," *Onde Electr.,* vol. 11, **pp.**230-240, June 1932.J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68-73.

[3] A. Blanchard, *Phase-Locked Loops: Application to Coherent Receiver Design.* New York: Wiley, 1976

[4] F. M. Gardner, *Phaselock Techniques,* 2nd ed. New York: Wiley, 1979.

[5] W. C. Lindsey and C. M. Chie, "A survey of digital phase-locked loops," *Proc. IEEE,* vol. 69, pp. 410-431, Apr. 1981.

[6] G. T. Volpe, "A phase-locked loop control system for a synchronous motor," ***IEEE Trans. Automat. Contr.,*** vol. AC-15, pp. 88-95, Feb. 1970

[7] B**.** K. Bose and K. **J.** Jentzen, "Digital speed control of a dc motor with PLL regulation," ***IEEE Ind. Electron. Contr. Instrum.,*** vol. IECI-25, pp.10-13, Feb. 1978.

[8] K. Eapen, K. Venkatesan, and **S.** C. Gupta, "Steady state and stability analysis of an analog-type phase-locked loop dc motor control system," ***IEEE Trans. Ind. Electron. Contr. Instrum.,*** vol. IECI-27, pp. 87-91, 1980.

[9] F. Harashima, H. Naitoh, M. Koyama, and **S.** Kondo, "Performance improvement in microprocessor-based digital PLL speed control system," ***IEEE Trans. Ind. Electron. Contr. Instrum.,*** vol. IECI-28, pp.5661,Feb. 1981.

[10] K. Eapen and K. Venkatesan, "Phase-locked loop dc motor drive with improved transient performance," ***IEEE Trans. Ind. EZectron. Contr. Instrum.,*** vol. IECI-28, pp. 347-352, Nov. 1981.

[11] D. F. Geiger, ***Phase Lock Loops for DC Motor Speed Control.*** New York Wiley, 1981.

[12] N. Margaris and V. Petridis, **"A** phase-locked regulator system study of a separately excited dc motor with triangular phase comparator," ***Int. J. Electron.,*** vol. 52, no. **3,** pp. 241-261, Mar. 1982.

[13] **"A** phase-locked regulator system study of a separately excited dc motor with phase-frequency comparator," ***Int. J. Electron.,*** vol. 52,no. 2, pp. 141-156, Feb. 1982.

[14] N. Margaris, **V.** Petridis, and D. Efthymiatos, "Phase-locked loop control of a nonlinear dc motor," ***IEEE Trans. Ind. Electron.,*** vol. IE-29, pp. 91-93, Feb. 1982.

[15] N. Margaris and V. Petridis, "PLL speed regulation of fractional horsepower series and universal motors," ***IEEE Trans. Ind. Electron.,*** vol. IE-31, pp. 277-281, Aug. 1984.

[16] "Voltage pump phase-locked loops," ***IEEE Trans. Ind. Electron.,***vol. IE-32, pp. 4149, Feb. 1985.

[17] G. C. Hsieh, Y. P. Wu, C. H. Lee, and C. H. Liu, "An adaptive digital pump controller for phase locked servo systems," ***IEEE Trans. Ind. Electron.,*** vol. IE-34, pp. 379-386, 1987.

[18] G. C. Hsieh, Y. **S.** Lin, and R. N. Jou, "A microprocessor-based Phaselocked servo system by slope-varied digital pumped technique," ***J.Chinese Inst. Eng.,*** vol. 15, no. **2,** pp. 405-414, 1992.

[19] G. C. Hsieh, "A study on position servo control systems by frequencylocked technique," ***IEEE Trans. Ind. Electron.,*** vol. 36, pp. 365-373,1989.

[20] J. C. Li and G. C. Hsieh, "A phase/frequency-locked controller forstepping servo systems," ***IEEE Trans. Ind. Electron.,*** vol. 39, pp. 379-386, Apr. 1992.

[21] M. F. Lai, ***G.*** C. Hsieh, and Y. P. Wu, "Variable slope pulse pump controller for stepping position servo control using frequency-locked technique," ***IEEE Trans. Ind. Electron.,*** vol. 42, pp. 29G299, June 1995.

[22] A. J. Goldstein, "Analysis to the phase controlled loop with a sawtooth comparator," *Bell Syst. Tech. J.,* pp. 603-633, 1963.

[23] R. C. E. Thomas, "Frequency comparator performs double duty," *EDN,* pp. 29-32, Nov. 1970.

[24] J. L. Brown, "A digital phase and frequency-sensitive detector," *Proc.* IEEE, vol. 59, p. 717, Apr. 1971.
[25] Phase-Locked Loop Datu Book, 2nd ed. Phoenix, AZ: Motorola, Aug. 1973.
[26] C. **A.** Sharpe, "A 3-state phase detector can improve your next PLL design," *EDN*, pp. 55-59, Sept. 1976.
[27] S. C. Gupta, K. Venkatesan, K. Eapen, and P. Pradhan, "A fast measuring phase detector for use in PLL motor control system," *IEEE Tran. Ind. Electron. Contr. Instrum.*, vol. IECI-25, pp. 75-76, 1978.
[28] F. M. Gardner, *Phaselock Techniques,* 2nd ed. New York: Wiley, 1979.
[29] L. J. Milligan and E. Carnicel, "Phase-locked loops provide accurate, efficient dc motor speed control," ***EDN,*** pp. 32-35, Aug. 1972.
[30] R. L. Labinger, "Designing phase-locked loop servos with digital IC's,'' ***Contr. Eng.,*** pp. 46-48, Feb. 1973.
[31] A. W. Moore, "Phase-locked loops for motor-speed control," ***IEEE Spectrum,*** pp. 61-67, Apr. 1973.
[32] D. H. Smithgall, "A phase-locked loop motor-control system," **IEEE Trans. Ind. Electron. Contr. Instrum.,** vol. IECI-22, pp. 487490, Nov.1975.
[33] H. E. Raphael, "Motor control by PLL," ***Electron. Des.,*** vol. 23, no. 9, pp. 54-57, Apr. 1975.
[34] H. Le-Huy and 0. L. Mercier, "A synchronous dc motor speed control system," **Proc. IEEE,** pp. 394-395, Mar. 1976.
[35] N. K. Sinha and N. H. Bailey, "Speed control of a dc servomoter using phase-locked loop: Some test results of a practical design," **IEEE Trans.**
[36] D. F. Geiger, ***Phase Lock Loops for DC Motor Speed Control.*** New York Wiley, 1981.
[37] A. Blanchard, *Phase-Locked Loops: Application to Coherent Receiver Design.* New York: Wiley, 1976.
[38] F. M. Gardner, *Phaselock Techniques,* 2nd ed. New York: Wiley, 1979.